



PATENT 2814

Case Docket No. MICRON.061DV1

Date: October 30, 2000

Page 1

In re application of : Ahmad
App. No. : 09/397,952
Filed : September 17, 1999
For : FABRICATION OF
INTEGRATED DEVICES
USING NITROGEN
IMPLANTATION
Examiner : Steven H. Rao
Art Unit : 2814

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on

October 30, 2000

(Date)
Adeel S. Akhtar
Adeel S. Akhtar, Reg. No. 41,349

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

Sir:

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated as shown below:

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CLAIMS AS FILED

	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADDITIONAL FEE
Total Claims	21 —	21	= 0 ×	\$18	= \$0
Independent Claims	4 —	4	= 0 ×	\$80	= \$0
If application has been amended to contain multiple dependent claim(s), then add				\$270	= \$0
Time Extension Fee					\$0
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT					\$0

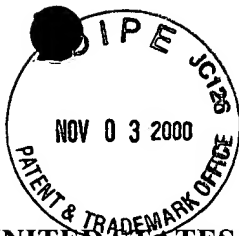
(X) Return prepaid postcard.

(X) Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410. A duplicate copy of this sheet is enclosed.

Adeel S. Akhtar
Adeel S. Akhtar
Registration No. 41,349
Attorney of Record

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MICRON.061DV1



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Ahmad) Group Art Unit 2814
Appl. No. : 09/397,952)
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(Date)
Adeel S. Akhtar, Reg. No. 41,394

AMENDMENT & RESPONSE TO OFFICE ACTION

Assistant Commissioner for Patents
Washington, D.C. 20231

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Dear Sir:

In response to the Office Action mailed August 2, 2000 in the above-captioned application, please amend the application as indicated below.

IN THE SPECIFICATION:

On page 1 of the specification, in the Reference to Related Application (added by Preliminary Amendment), after "filed June 9, 1997" insert -

Patent No. 6,037,639

IN THE CLAIMS:

1. (Amended) A process of forming a gate structure on a semiconductor substrate, comprising:

providing a semiconductor substrate having a channel region formed therein so as to define a source and a drain region and a gate structure comprised of a gate dielectric positioned on said channel region and a conductive layer positioned on said gate dielectric;